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EXAMINER	
SHAPIRO, LEONID	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding..

Office Action Summary	Application No. 10/697,471	Applicant(s) LEE ET AL.	
	Examiner Leonid Shapiro	Art Unit 2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Objections

1. Claims 1-20 objected to because of the following informalities:

All abbreviations in claims need to be decipher.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Limitations of independent claims 1,11,15,16 related to **Optically** Compensated Birefringence (OCB) mode, which is confusing, because Applicant's subject matter contain only **electrically** controlled LCD.

As to claims 5,20 it is not clear how the bias voltage could be **current voltage**?

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1,5-8,10,15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. (US Patent No. 6,069,620) in view of Nakao et al. (US patent No. 6,933,916 B2).

As to claim 1, Nakamura et al. teaches a liquid crystal display comprising:

a liquid crystal display panel having an array substrate on which a scan line and a data line are formed, a color filter substrate on which a common electrode is formed, and a liquid crystal layer interposed between the array and color filter substrates and operated in an OCB mode (See Col. 1, Lines 7-12, Fig. 6, items 2-4, Col. 6, Lines 1-9);

Notice, that color filter inherently will be placed on common electrode for TFT displays at the time of the invention (See for example US Patent No. 7,023,416 B1, Fig. 10, items 2,12, Col. 10, Lines 52-60); .

a source driver to supply an image signal to the data line (Fig. 1, item 14, Col. 4, Lines 16-23);

a scan driver to supply a scan signal to the scan line (Fig. 1, item 14); and

a controller, responsive to a power source, to control a bias voltage to be supplied to the common electrode, which has a voltage level higher than that of a common voltage supplied to the common electrode, so as to improve a transition speed of the liquid crystal layer into a bend alignment state, to control the common voltage to be supplied to the common electrode when the liquid crystal layer is transited into the bend alignment state so as to display an image using the image signal (See Fig. 6, items 40-48, Col. 5, Lines 51-67 and Fig. 7, item t1, Col. 6, Lines 33-52).

Nakamura teaches a common electrode line. Nakamura, col. 3, line 67 – col. 4, line 4. Nakamura teaches that the common electrode line [common electrode] receives the bias voltage [10V-30V] at an initial operation [period t1 when the power-on reset signal is output for t1 seconds] of the LCD. Nakamura, col. 6, lines 34 – 43; and figure 7. In the embodiment shown in figure 7, the voltage is applied to both the common electrode and the storage capacitance electrode. Nakamura teaches, however, that the bias voltage may be applied exclusively to the common electrode.

> Although in this embodiment voltages are applied to both of the common electrode and the storage capacitance lines, a modification is possible in which a voltage is applied to one of those, for instance, the common electrode but no voltages are applied to the storage capacitance lines.

Nakamura, col. 7, lines 1 – 5.

Nakamura et al. does not disclose to control the bias voltage to be supplied to the common electrode when the image signal is not input so as to maintain the bend alignment state of the liquid crystal layer.

Nakao et al. teaches to control the bias voltage to be supplied to the common electrode when the image signal is not input so as to maintain the bend alignment state of the liquid crystal layer (See Fig. 41, item 168, Col. 30, Lines 6-9 and 61-65).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Nakao et al. into Nakamura et al. system in order to reduce start time (See Col. 30. Lines 6-9).

As to claims 5-6, Nakamura et al. teaches the bias voltage is an alternating square wave voltage (See Fig. 7, items t1, COMMON ELECTRODE).

As to claim 7 Nakamura et al. teaches generated from a power source (See Fig. 6,item 46).

As to claim 8 Nakamura et al. teaches controller controls the common voltage and the bias voltage to be alternately supplied to the common electrode in response to the power source (See Fig. 6, items 40-46, Col. 5, Lines 51-67).

As to claim 10 Nakamura et al. teaches the bias voltage is supplied to the common electrode for a first time so as to transit the liquid crystal layer into the bend alignment state and the common voltage is supplied to the common electrode after the first time so as to display the image on the liquid crystal display panel (See Fig. 7, items t1, COMMON ELECTRODE).

As to claim 15, Nakamura et al. teaches an apparatus for driving a liquid crystal display including an array substrate on which a scan line and a data line are formed, a color filter substrate on which a common electrode is formed, and a liquid crystal layer interposed between the array and color filter substrates and operated in an OCB mode (See Col. 1, Lines 7-12, Fig. 6, items 2-4, Col. 6, Lines 1-9);

Notice, that color filter inherently will be placed on common electrode substrate for TFT displays at the time of the invention (See for example US Patent No. 7,023,416 B1, Fig. 10, items 2,12, Col. 10, Lines 52-60); .

a source driver to supply an image signal to the data line (Fig. 1, item 14, Col. 4, Lines 16-23);

a scan driver to supply a scan signal to the scan line (Fig. 1, item 14); and

a controller, responsive to a power source, to control a bias voltage to be supplied to the common electrode, which has a voltage level higher than that of a common voltage supplied to the common electrode, so as to improve a transition speed of the liquid crystal layer into a bend alignment state, to control the common voltage to be supplied to the common electrode when the liquid crystal layer is transited into the bend alignment state so as to display an image using the image signal (See Fig. 6, items 40-48, Col. 5, Lines 51-67 and Fig. 7, item t1, Col. 6, Lines 33-52).

Nakamura teaches a common electrode line. Nakamura, col. 3, line 67 – col. 4, line 4. Nakamura teaches that the common electrode line [common electrode] receives the bias voltage [10V-30V] at an initial operation [period t1 when the power-on reset signal is output for t1 seconds] of the LCD. Nakamura, col. 6, lines 34 – 43; and figure 7. In the embodiment shown in figure 7, the voltage is applied to both the common electrode and the storage capacitance electrode. Nakamura teaches, however, that the bias voltage may be applied exclusively to the common electrode.

> Although in this embodiment voltages are applied to both of the common electrode and the storage capacitance lines, a modification is possible in which a voltage is applied to one of those, for instance, the common electrode but no voltages are applied to the storage capacitance lines.

Nakamura, col. 7, lines 1 – 5.

Nakamura et al. does not disclose to control the bias voltage to be supplied to the common electrode when the image signal is not input so as to maintain the bend alignment state of the liquid crystal layer.

Nakao et al. teaches to control the bias voltage to be supplied to the common electrode when the image signal is not input so as to maintain the bend alignment state of the liquid crystal layer (See Fig. 41, item 168, Col. 30, Lines 6-9 and 61-65).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Nakao et al. into Nakamura et al. system in order to reduce start time (See Col. 30. Lines 6-9).

4. Claims 9, 16, 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. in view of Nakao et al. and Tanaka et al. (US Patent No. 6,121,945).

As to claim 16, Nakamura et al. teaches a liquid crystal display comprising:

a liquid crystal display panel having an array substrate on which a scan line and a data line are formed, a color filter substrate on which a common electrode is formed, and a liquid crystal layer interposed between the array and color filter substrates and operated in an OCB mode (See Col. 1, Lines 7-12, Fig. 6, items 2-4, Col. 6, Lines 1-9);

a source driver to supply an image signal to the data line (Fig. 1, item 14, Col. 4, Lines 16-23);

a scan driver to supply a scan signal to the scan line (Fig. 1, item 14);

a switching part that receives the bias voltage and common voltage (See Fig. 6, items Vcom, Vcs, 44, Col. 5, Lines 51-67) having a second voltage level lower that the first voltage level (See Fig. 7) and outputs the bias voltage or the common voltage in

response to the third control signal (power-on signal) (See Fig. 6, items Vcom, Vcs, 44,46,48 Col. 5, Lines 51-67), and

a controller that receives a power signal and the image signal, supplies the third control signal to the switching part in response to the power signal so as to apply the bias voltage to the common electrode during a predetermined first time, supplies the first, second and fourth control signals to the source driver, scan driver and switching part in response to the image signal (See Fig. 6, items 40-48, Col. 5, Lines 51-67 and Fig. 7, item t1, Col. 6, Lines 33-52).

Nakamura teaches a common electrode line. Nakamura, col. 3, line 67 – col. 4, line 4. Nakamura teaches that the common electrode line [common electrode] receives the bias voltage [10V-30V] at an initial operation [period t1 when the power-on reset signal is output for t1 seconds] of the LCD. Nakamura, col. 6, lines 34 – 43; and figure 7. In the embodiment shown in figure 7, the voltage is applied to both the common electrode and the storage capacitance electrode. Nakamura teaches, however, that the bias voltage may be applied exclusively to the common electrode.

> Although in this embodiment voltages are applied to both of the common electrode and the storage capacitance lines, a modification is possible in which a voltage is applied to one of those, for instance, the common electrode but no voltages are applied to the storage capacitance lines.

Nakamura, col. 7, lines 1 – 5.

Nakamura et al. does not disclose to supply the common voltage to the common electrode after the predetermined first time, and supplies the third control signal to the switching part when the image signal is not input so as to supply the bias voltage to the common electrode and fourth control signal.

Nakao et al. teaches to control the bias voltage to be supplied to the common electrode when the image signal is not input so as to maintain the bend alignment state of the liquid crystal layer (See Fig. 41, item 168, Col. 30, Lines 6-9 and 61-65) and fourth control signal (when backlight is turn on/off) (See Fig. 41, item 168, Col. 29, Lines 53-62).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Nakao et al. into Nakamura et al. system in order to reduce start time (See Col. 30. Lines 6-9).

Nakao et al. and Nakamura et al. do not disclose a DC-DC converter that generates the bias voltage having a first voltage level.

Tanaka et al. teaches a DC-DC converter that generates the bias voltage (See Fig. 7, items VH,VL, Col. 9, Lines 5-10).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Tanaka et al. into Nakao et al. and Nakamura et al. system in order to improve display quality (See Col. 2, Lines 66-67 in Tanaka et al reference).

As to claim 9, Tanaka et al. teaches a DC-DC converter that generates the bias voltage (See Fig. 7, items VH,VL, Col. 9, Lines 5-10) and Nakamura teaches a switching part that receives the bias voltage and common voltage (See Fig. 6, items Vcom, Vcs, 44, Col. 5, Lines 51-67) having a second voltage level lower that the first voltage level (See Fig. 7) and outputs the bias voltage or the common voltage in

response to the third control signal (power-on signal) (See Fig. 6, items Vcom, Vcs, 44,46,48 Col. 5, Lines 51-67).

As to claim 19, Nakao et al. teaches to control the bias voltage to be supplied to the common electrode when the image signal is not input so as to maintain the bend alignment state of the liquid crystal layer (See Fig. 41, item 168, Col. 30, Lines 6-9 and 61-65) and fourth control signal (when backlight is turn on/off) (See Fig. 41, item 168, Col. 29, Lines 53-62).

As to claim 20, Nakamura et al. teaches the bias voltage is an alternating square wave voltage (See Fig. 7, items t1, COMMON ELECTRODE).

5. Claims 2-4, 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable Nakamura et al. in view of Nakao et al. and Kempisty (Pub. No.: US 2003/0169234 A1).

As to claim 11, Nakamura et al. teaches a method of driving a liquid crystal display including a liquid crystal display panel operated in an OCB mode (See Col. 1, Lines 7-12, Fig. 6, items 2-4, Col. 6, Lines 1-9), a liquid crystal display module having a scan driver and a source driver (See Fig. 1, item 14,16), and a backlight assembly disposed under the liquid crystal display panel (See Col. 7, Lines 47-64), comprising

responsive to a power source, to control a bias voltage to be supplied to the common electrode so as to improve a transition speed of the liquid crystal layer into a bend alignment state such that the liquid crystal is operated in the OCB mode, displaying an image after the liquid crystal is transient into the bend alignment state (See Fig. 6, items 40-48, Col. 5, Lines 51-67 and Fig. 7, item t1, Col. 6, Lines 33-52).

Nakamura teaches a common electrode line. Nakamura, col. 3, line 67 – col. 4, line 4. Nakamura teaches that the common electrode line [common electrode] receives the bias voltage [10V-30V] at an initial operation [period t1 when the power-on reset signal is output for t1 seconds] of the LCD. Nakamura, col. 6, lines 34 – 43; and figure 7. In the embodiment shown in figure 7, the voltage is applied to both the common electrode and the storage capacitance electrode. Nakamura teaches, however, that the bias voltage may be applied exclusively to the common electrode.

> Although in this embodiment voltages are applied to both of the common electrode and the storage capacitance lines, a modification is possible in which a voltage is applied to one of those, for instance, the common electrode but no voltages are applied to the storage capacitance lines.

Nakamura, col. 7, lines 1 – 5.

Nakamura et al. does not disclose to checking whether or not a data signal for the image is inputted; displaying the image when the data signal is inputted; checking whether or not a first time passes when the data signal is not inputted;.

Nakao et al. teaches to control the bias voltage to be supplied to the common electrode when the image signal is not input so as to maintain the bend alignment state of the liquid crystal layer (See Fig. 41, item 168, Col. 30, Lines 6-9 and 61-65).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Nakao et al. into Nakamura et al. system in order to reduce start time (See Col. 30. Lines 6-9).

Nakamura et al. and Nakao et al. do not disclose displaying an OSD representing that the data signal is not inputted when the first time passes; controlling the liquid crystal to be transited into the bend alignment state while the

OSD is displayed; checking whether or not the data signal for the image is inputted; and displaying the image after canceling the OSD when the data signal is input.

Kempisty teaches to display default content (OSD) where no input data is provided for predetermined period (timeout) (See Fig. 4, items 406,408,410, paragraph 0054).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Kempisty into Nakao et al. and Nakamura et al. system in order to include OSD (See paragraph 0001 in the Kempisty reference).

As to claims 12-13, Nakamura et al. teaches cutting of the bias voltage supplied to the liquid crystal display panel successively supplying a common voltage to the liquid crystal display panel when the first time passes (See Fig. 7, after t1); supplying a driving voltage to the backlight assembly with the common voltage supplied to the liquid crystal display panel (See Col. 7, Lines 47-64); and supplying an image signal and a scan signal for the OSD to the liquid crystal display panel (See Fig. 6, items Vg,Vd, Col. 6, Lines 15-25).

As to claims 2-4, 14 Kempisty teaches the controller controls an OSD to be displayed on the liquid crystal display panel before the bend alignment state of the liquid crystal layer is broken down when the image signal is not inputted (See Fig. 4, items 406,408,410, paragraph 0054) and Nakao et al. teaches the controller controls voltage to be supplied to the common electrode (See Fig. 41, item 168, Col. 30, Lines 6-9 and 61-65) while the OSD is displayed on the liquid crystal display panel (See Fig. 4, items 406,408,410, paragraph 0054).

6. Claims 17-18 rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al., Nakao et al. and Tanaka et al. as applied to claim 16 above, and further in view of Kempisty.

Nakamura et al., Nakao et al. and Tanaka et al. do not disclose the controller controls an OSD to be displayed on the liquid crystal display panel before the bend alignment state of the liquid crystal layer is broken down when the image signal is not inputted, the controller controls voltage to be supplied to the common electrode while the OSD is displayed on the liquid crystal display panel.

Kempisty teaches the controller controls an OSD to be displayed on the liquid crystal display panel before the bend alignment state of the liquid crystal layer is broken down when the image signal is not inputted (See Fig. 4, items 406,408,410, paragraph 0054) and Nakao et al. teaches the controller controls voltage to be supplied to the common electrode (See Fig. 41, item 168, Col. 30, Lines 6-9 and 61-65) while the OSD is displayed on the liquid crystal display panel (See Fig. 4, items 406,408,410, paragraph 0054).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Kempisty into Nakao et al. and Nakamura et al., Tanaka et al. system in order to include OSD (See paragraph 0001 in the Kempisty reference).

Telephone Inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 571-272-7683. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LS
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